Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrolment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2019

CS3CO22 Computer System Architecture

Programme: B.Tech. Branch/Specialisation: CS

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Which of the following statements is correct? **1**

I. Bus is a group of information carrying wires.
II. Bus is needed to achieve reasonable speed of operation.
III. Bus can carry data or address.
IV. A bus can be shared by more than one device.

(a) I and II only (b) I, II and III only
(c) II, III and IV only (d) All of these.

ii. Unit of computer which is capable of performing arithmetic, logical and data manipulation operations on binary numbers is called? **1**

(a) CU (b) ALU (c) I/O unit (d) Processing unit

iii. The instruction, Add #45, R1 does _____ **1**

(a) Adds the value of 45 to the address of R1 and stores 45 in that address
(b) Adds 45 to the value of R1 and stores it in R1
(c) Finds the memory location 45 and adds that content to that of R1
(d) None of these

iv. _____is the sequence of operations performed by CPU in processing an instruction: **1**

(a) Execute cycle (b) Fetch cycle
(c) Decode (d) Instruction cycle

v. A subtractor is not usually present in a computer because **1**

(a) It is expensive
(b) It is not possible to design it
(c) The adder will take care of subtraction
(d) None of these

P.T.O.

vi. A negative number cannot be represented in: **1**
(a) Signed magnitude form (b) 1's compliment form
(c) 2's compliment form (d) None of these

vii. LRU stands for _____ **1**
(a) Low Rate Usage (b) Least Rate Usage
(c) Least Recently Used (d) Low Required Usage

viii. The data transmission which uses a clock to control timing of bit being sent is **1**
(a) Synchronous (b) Parallel
(c) Synchronous serial (d) None of these

ix. Which of the following are typical characteristics of a RISC machine? **1**
I. Instruction taking multiple cycles
II. Highly pipelined
III. Instructions interpreted by microprograms
IV. Multiple register sets.
(a) II and IV only (b) I and III only
(c) I, II and III only (d) All of these

x. If the stage delay of 5-stage pipelined processor is 1,2,3,2,1 respectively than throughput of processor is _____. **1**
(a) $\frac{1}{3}$ (b) $\frac{1}{9}$ (c) $\frac{1}{7}$ (d) None of these

Q.2 i. List the major differences between Computer Organization and Computer Architecture. **2**

ii. Explain the register transfer language and the basic symbols used in register transfer. **3**

iii. What is bus? Draw the figure to show how functional units are interconnected using a bus and explain it. **5**

OR iv. What is meant by Arithmetic Micro-operations? List and explain the different Arithmetic Micro-operations with an example. **5**

Q.3 i. With an example of each, explain memory reference instructions? **2**

ii. What do you mean by the term addressing modes? List any six addressing modes with one example for each. **8**

OR iii. Define interrupt. Explain any six different types of interrupts. **8**

Q.4 i. Explain 2's complement method of subtraction of binary numbers. **3**

ii. Explain Booth's algorithm for multiplication of two fixed point numbers. Take two numbers of your choice for explaining the multiplication process. **7**

OR iii. Draw flowchart to explain division algorithm for signed magnitude data. What is divide overflow condition? **7**

Q.5 i. Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. **4**

ii. Define the following: **6**
(a) Associative Memory (b) Virtual Memory
(c) Synchronous Data transfer

OR iii. What is cache mapping? Explain any of the cache mapping technique with neat and clean diagram. **6**

Q.6 Attempt any two:

i. List the characteristics of RISC and CISC processors. **5**

ii. What is meant by Flynn's classification? Explain **5**

iii. What is pipelining and what is its advantages? **5**

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Marking Scheme
CS3CO22 Computer System Architecture

Q.1	i.	Which of the following statements is correct? I. Bus is a group of information carrying wires. II. Bus is needed to achieve reasonable speed of operation. III. Bus can carry data or address. IV. A bus can be shared by more than one device. (d) All of these.		**1**
	ii.	Unit of computer which is capable of performing arithmetic, logical and data manipulation operations on binary numbers is called? (b) ALU		**1**
	iii.	The instruction, Add #45, R1 does _____ (b) Adds 45 to the value of R1 and stores it in R1		**1**
	iv.	_____is the sequence of operations performed by CPU in processing an instruction: (d) Instruction cycle		**1**
	v.	A subtractor is not usually present in a computer because (c) The adder will take care of subtraction		**1**
	vi.	A negative number cannot be represented in: (d) None of these		**1**
	vii.	LRU stands for _____ (c) Least Recently Used		**1**
	viii.	The data transmission which uses a clock to control timing of bit being sent is (a) Synchronous		**1**
	ix.	Which of the following are typical characteristics of a RISC machine? I. Instruction taking multiple cycles II. Highly pipelined III. Instructions interpreted by microprograms IV. Multiple register sets. (a) II and IV only		**1**
	x.	If the stage delay of 5-stage pipelined processor is 1,2,3,2,1 respectively than throughput of processor is _____. (a) $\frac{1}{3}$		**1**
Q.2	i.	Differences between Computer Organization and Computer Architecture. (4 Points)	(0.5 mark*4)	**2**
	ii.	Register transfer language Basic symbols	1.5 marks 1.5 marks	**3**
	iii.	Bus definition Diagram Explanation	1 mark 2 marks 2 marks	**5**
OR	iv.	Arithmetic Micro-operations List and explanation	1 mark 4 marks	**5**
Q.3	i.	With an example of each, Memory reference instructions (As per answer)	2 marks	**2**
	ii.	Addressing modes List any six addressing modes Example for each addressing modes.	2 marks 3 marks 3 marks	**8**
OR	iii.	Definition interrupt Any six different types of interrupts.	2 marks 6 marks	**8**
Q.4	i.	Explain 2's complement method of subtraction of binary numbers. (As per answers)	3 marks	**3**
	ii.	Booth's Algorithm+ Flow chart Example for explaining the multiplication process	3 marks 4 marks	**7**
OR	iii.	Flowchart Overflow condition	5 marks 2 marks	**7**
Q.5	i.	Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer)	4 marks	**4**
	ii.	Define the following: (a) Associative Memory (b) Virtual Memory (c) Synchronous Data transfer	2 marks 2 marks 2 marks	**6**
OR	iii.	Cache mapping Explanation with diagram.	2 marks 4 marks	**6**
Q.6		Attempt any two:		
	i.	Characteristics of RISC (Minimum 5 points) Characteristics of CISC (Minimum 5 points)	2.5 marks 2.5 marks	**5**
	ii.	Flynn's classification Explain	1 mark 4 marks	**5**
	iii.	Define pipelining Advantages	3 marks 2 marks	**5**

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