Total No. of Questions: 6

Total No. of Printed Pages:3

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Enrolment No.....

Faculty of Engineering End Sem (Odd) Examination Dec-2019 CS3CO22 Computer System Architecture

Branch/Specialisation: CS Programme: B.Tech.

Duration: 3 Hrs. Maximum Marks: 60

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of

Q.1 (MCQs) should be written in full instead of only a, b, c or d. Which of the following statements is correct? Q.1 i. 1 I. Bus is a group of information carrying wires. II. Bus is needed to achieve reasonable speed of operation. III. Bus can carry data or address. IV. A bus can be shared by more than one device. (a) I and II only (b) I, II and III only (c) II, III and IV only (d) All of these. Unit of computer which is capable of performing arithmetic, logical and 1 data manipulation operations on binary numbers is called? (a) CU (b) ALU (c) I/O unit (d) Processing unit The instruction, Add #45, R1 does _____ 1 (a) Adds the value of 45 to the address of R1 and stores 45 in that address (b) Adds 45 to the value of R1 and stores it in R1 (c) Finds the memory location 45 and adds that content to that of **R**1 (d) None of these _____is the sequence of operations performed by CPU in processing an 1 iv. instruction: (a) Execute cycle (b) Fetch cycle (c) Decode (d) Instruction cycle A subtractor is not usually present in a computer because 1 (a) It is expensive (b) It is not possible to design it (c) The adder will take care of subtraction (d) None of these

P.T.O.

[2]

	vi.	A negative number cannot be represented in:	1	
		(a) Signed magnitude form (b) 1's compliment form		
		(c) 2's compliment form (d) None of these		
	vii.	LRU stands for	1	
	, 11,	(a) Low Rate Usage (b) Least Rate Usage		
		(c) Least Recently Used (d) Low Required Usage		
	viii.	The data transmission which uses a clock to control timing of bit being	1	
		sent is		
		(a) Synchronous (b) Parallel		
		(c) Synchronous serial (d) None of these		
	ix.	Which of the following are typical characteristics of a RISC machine?	1	
		I. Instruction taking multiple cycles		
		II. Highly pipelined		
		III. Instructions interpreted by microprograms		
		IV. Multiple register sets.		
		(a) II and IV only (b) I and III only		
		(c) I, II and III only (d) All of these		
	х.	If the stage delay of 5-stage pipelined processor is 1,2,3,2,1 respectively	1	
	71.	than throughput of processor is		
		(a) $\frac{1}{3}$ (b) $\frac{1}{9}$ (c) $\frac{1}{7}$ (d) None of these		
		(a) $\frac{1}{3}$ (b) $\frac{1}{9}$ (c) $\frac{7}{7}$ (d) Notice of these		
0.2		List the major life and hat a Committee Committee and	2	
Q.2	i.	List the major differences between Computer Organization and	2	
		Computer Architecture.	3	
	ii.			
	:::	register transfer. What is bus? Draw the figure to show how functional units are	5	
	iii.	interconnected using a bus and explain it.		
OR iv.	iv.	What is meant by Arithmetic Micro-operations? List and explain the	5	
OK IV.		different Arithmetic Micro-operations with an example.	3	
		different / tritimiette (vitero-operations with an example.		
Q.3	i.	With an example of each, explain memory reference instructions?	2	
Q .5	ii.	What do you mean by the term addressing modes? List any six addressing 8		
	11.	modes with one example for each.		
OR	iii.	Define interrupt. Explain any six different types of interrupts.	8	
J1 X	111.	Define interrupt. Displain any six different types of interrupts.	J	
		[3]		
		r- 1		
Q.4	i.	Explain 2's complement method of subtraction of binary numbers.	3	

	ii.	Explain Booth's algorithm for multiplication of two fixed point numbers. Take two numbers of your choice for explaining the multiplication process.	7
OR	iii.	Draw flowchart to explain division algorithm for signed magnitude data. What is divide overflow condition?	7
Q.5	i.	Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames.	4
	ii.	Define the following: (a) Associative Memory (b) Virtual Memory (c) Synchronous Data transfer	6
OR	iii.	What is cache mapping? Explain any of the cache mapping technique with neat and clean diagram.	6
Q.6		Attempt any two:	
	i.	List the characteristics of RISC and CISC processors.	5
	ii.	What is meant by Flynn's classification? Explain	5
	iii.	What is pipelining and what is its advantages?	5

Marking Scheme CS3CO22 Computer System Architecture

2.1	i.	Which of the following statements is correct?		1
		I. Bus is a group of information carrying wires.		
		II. Bus is needed to achieve reasonable speed of	operation.	
		III. Bus can carry data or address.		
		IV. A bus can be shared by more than one device.		
		(d) All of these.		
	ii.	Unit of computer which is capable of performing ari data manipulation operations on binary numbers is call (b) ALU	_	1
	iii.	The instruction, Add #45, R1 does		1
	111.	(b) Adds 45 to the value of R1 and stores it in R1		•
	iv.	is the sequence of operations performed by Clinstruction:	PU in processing an	1
		(d) Instruction cycle		
	v.	A subtractor is not usually present in a computer becau	ise	1
		(c) The adder will take care of subtraction		
	vi.	A negative number cannot be represented in:		1
		(d) None of these		1
	vii.	LRU stands for (c) Least Recently Used		1
	viii.	The data transmission which uses a clock to control	timing of hit being	1
	V 1111.	sent is	timing or oil being	•
		(a) Synchronous		
	ix.	Which of the following are typical characteristics of a	RISC machine?	1
		I. Instruction taking multiple cycles		
		II. Highly pipelined		
		III. Instructions interpreted by microprograms		
		IV. Multiple register sets.		
		(a) II and IV only	2221	
	х.	If the stage delay of 5-stage pipelined processor is 1	,2,3,2,1 respectively	1
		than throughput of processor is		
		(a) $\frac{1}{3}$		
0.2	i.	Differences between Computer Organization	and Computer	2
		Architecture. (4 Points)	(0.5 mark*4)	
	ii.	Register transfer language	1.5 marks	3
		Basic symbols	1.5 marks	
	iii.	Bus definition	1 mark	5
		Diagram	2 marks	
		Explanation	2 marks	

Q.3 i. With an example of each, Memory reference instructions (As per answer) 2 marks ii. Addressing modes 2 marks 2 marks Example for each addressing modes. 3 marks Example for each addressing modes. 3 marks OR iii. Definition interrupt 2 marks Any six different types of interrupts. 6 marks Q.4 i. Explain 2's complement method of subtraction of binary numbers. (As per answers) 3 marks ii. Booth's Algorithm+ Flow chart Example for explaining the multiplication process 4 marks OR iii. Flowchart Overflow condition 2 marks Q.5 i. Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) 4 marks ii. Define the following: (a) Associative Memory 2 marks (b) Virtual Memory 2 marks	OR	iv.	Arithmetic Micro-operations	1 mark	5
(As per answer) ii. Addressing modes List any six addressing modes Example for each addressing modes. OR iii. Definition interrupt 2 marks Any six different types of interrupts. OR iii. Explain 2's complement method of subtraction of binary numbers. (As per answers) 3 marks ii. Booth's Algorithm+ Flow chart Example for explaining the multiplication process 4 marks OR iii. Flowchart Overflow condition 7 Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) 4 marks ii. Define the following: (a) Associative Memory 2 marks 6			List and explanation	4 marks	
(As per answer) ii. Addressing modes List any six addressing modes Example for each addressing modes. OR iii. Definition interrupt 2 marks Any six different types of interrupts. OR iii. Explain 2's complement method of subtraction of binary numbers. (As per answers) 3 marks ii. Booth's Algorithm+ Flow chart Example for explaining the multiplication process 4 marks OR iii. Flowchart Overflow condition 7 Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) 4 marks ii. Define the following: (a) Associative Memory 2 marks 6					
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OR iii. Definition interrupt Any six different types of interrupts. Q.4 i. Explain 2's complement method of subtraction of binary numbers. (As per answers) 3 marks ii. Booth's Algorithm+ Flow chart Example for explaining the multiplication process 4 marks OR iii. Flowchart Overflow condition Q.5 i. Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) 4 marks ii. Define the following: (a) Associative Memory 2 marks 6			List any six addressing modes	3 marks	
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Q.4 i. Explain 2's complement method of subtraction of binary numbers. (As per answers) 3 marks ii. Booth's Algorithm+ Flow chart 3 marks Example for explaining the multiplication process 4 marks OR iii. Flowchart 5 marks Overflow condition 2 marks Q.5 i. Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) 4 marks ii. Define the following: (a) Associative Memory 2 marks	OR	iii.	Definition interrupt	2 marks	8
(As per answers) ii. Booth's Algorithm+ Flow chart Example for explaining the multiplication process OR iii. Flowchart Overflow condition 2 marks Q.5 i. Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) ii. Define the following: (a) Associative Memory 3 marks 7 7 7 8 9 10 11 12 13 14 15 15 15 16 16 16 17 18 19 19 10 10 10 10 10 10 10 10			Any six different types of interrupts.	6 marks	
ii. Booth's Algorithm+ Flow chart 3 marks Example for explaining the multiplication process 4 marks OR iii. Flowchart 5 marks Overflow condition 2 marks Q.5 i. Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) 4 marks ii. Define the following: 6 (a) Associative Memory 2 marks	Q.4	i.	Explain 2's complement method of subtraction of bina	ry numbers.	3
Example for explaining the multiplication process 4 marks OR iii. Flowchart 5 marks Overflow condition 2 marks Q.5 i. Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) 4 marks ii. Define the following: 6 (a) Associative Memory 2 marks			(As per answers)	3 marks	
OR iii. Flowchart 5 marks 7 Overflow condition 2 marks Q.5 i. Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) 4 marks ii. Define the following: 6 (a) Associative Memory 2 marks		ii.	Booth's Algorithm+ Flow chart	3 marks	7
Overflow condition 2 marks Q.5 i. Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) 4 marks ii. Define the following: (a) Associative Memory 2 marks			Example for explaining the multiplication process	4 marks	
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Find the number of page faults using LRU page replacement algorithm with 3 page frames. (As per answer) 4 marks ii. Define the following: (a) Associative Memory 2 marks			Overflow condition	2 marks	
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with 3 page frames. (As per answer) ii. Define the following: (a) Associative Memory 4 marks 6 2 marks	Q.5	i.	Consider the following reference strings: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5		
ii. Define the following: 6 (a) Associative Memory 2 marks			Find the number of page faults using LRU page replacement algorithm		
(a) Associative Memory 2 marks			with 3 page frames. (As per answer)	4 marks	
•		ii.	Define the following:		6
(b) Virtual Memory 2 marks			(a) Associative Memory	2 marks	
(0)			(b) Virtual Memory	2 marks	
(c) Synchronous Data transfer 2 marks			(c) Synchronous Data transfer	2 marks	
OR iii. Cache mapping 2 marks 6	OR	iii.		2 marks	6
Explanation with diagram. 4 marks			Explanation with diagram.	4 marks	
Q.6 Attempt any two:	Q.6		Attempt any two:		
i. Characteristics of RISC (Minimum 5 points) 2.5 marks 5		i.	Characteristics of RISC (Minimum 5 points)	2.5 marks	5
Characteristics of CISC (Minimum 5 points) 2.5 marks			Characteristics of CISC (Minimum 5 points)	2.5 marks	
ii. Flynn's classification 1 mark 5		ii.		1 mark	5
Explain 4 marks			Explain	4 marks	
iii. Define pipelining 3 marks 5		;;;	-	3 marks	5
Advantages 2 marks		111.		0 111011110	
